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(54) Title: ACTIVE GUARDING FOR REDUCTION OF RESISTIVE AND CAPACTIVE SIGNAL LOADING WITH ADJUSTABLE CONTROL OF COMPENSATION LEVEL

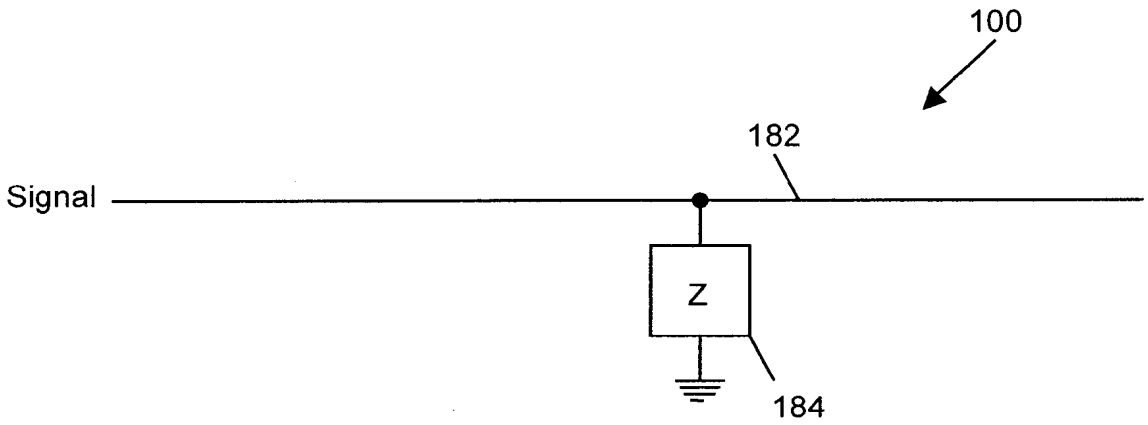

FIG. 1

(57) Abstract: In various embodiments, applicants' teachings are related to an active guarding circuit and method for reducing parasitic impedance signal loading on a signal-transmission channel that is shunted by a parasitic impedance. The presence of an electrical signal on the signal-transmission channel causes a leakage current to flow through the parasitic impedance. In various embodiments, the circuit comprises an amplifier and an impedance, one terminal of the impedance is coupled to the signal-transmission channel. The input of the amplifier is coupled to the signal-transmission channel and the output is coupled to the other terminal of the impedance so as to cause a compensation current to flow through the impedance. The gain of the amplifier and the value of the impedance are selected so that the compensation current has a magnitude substantially equal to the leakage current magnitude.

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TITLE: ACTIVE GUARDING FOR REDUCTION OF RESISTIVE AND CAPACITIVE SIGNAL LOADING WITH ADJUSTABLE CONTROL OF COMPENSATION LEVEL

[0001] The section headings used herein are for organizational purposes only and are not to be construed as limiting the subject matter described in any way.

FIELD

[0002] Applicants' teachings are related to a method and circuit for reducing resistive and capacitive signal loading.

SUMMARY

[0003] In various embodiments, applicants' teachings relate to an active guarding circuit for reducing parasitic impedance signal loading. In various embodiments, the circuit comprises a signal-transmission channel, an impedance, and an amplifier. The signal-transmission channel carries an electrical signal and is shunted by a parasitic impedance having a parasitic impedance value. The electrical signal causes a leakage current having a leakage current magnitude to flow through the parasitic impedance. The impedance has an impedance value, a first terminal and a second terminal; the first terminal is coupled to the signal-transmission channel. The amplifier has an input terminal, an output terminal and a gain. The input terminal of the amplifier is coupled to the signal-transmission channel, the output terminal of the amplifier is coupled to the second terminal of the impedance to provide a compensation current to flow through the impedance, and the gain is selected based on the impedance and parasitic impedance values so that the compensation current has a magnitude substantially equal to the leakage current magnitude.

[0004] In some embodiments, the impedance is the parasitic impedance. In various other embodiments, the impedance is separate from the parasitic impedance.

[0005] In various embodiments, the gain of the amplifier is substantially equal to 1.

[0006] The active guarding circuit as defined in claim 4, wherein the gain and the compensation impedance are selected so that the compensation current magnitude is substantially equal to the leakage current magnitude.

[0007] In some embodiments, the gain of the amplifier is greater than 1.

[0008] In various embodiments, the impedance includes a capacitance. In some embodiments, the impedance includes a resistance. In some embodiments, the impedance includes both a resistance and a capacitance. In various other embodiments, the impedance is a capacitance. In some other embodiments, the impedance is a resistance.

[0009] In various embodiments, applicants' teachings relate to a method of active guarding for reducing parasitic impedance signal loading. The method comprises sensing an electrical signal on the signal-transmission channel, the signal-transmission channel is shunted by a parasitic impedance having a parasitic impedance value, the electrical signal causing a leakage current having a leakage current magnitude to flow through the parasitic impedance. The method further comprises providing an impedance having an impedance value, with a first terminal and a second terminal, the first terminal is coupled to the signal-transmission channel. The method further comprises providing an amplified signal to the second terminal of the impedance to cause a compensation current to flow through the impedance, the amplified signal is equal to the electrical signal multiplied by a gain, the gain is selected based on the impedance value and the parasitic impedance value so that the magnitude of the compensation current is substantially equal to the leakage current magnitude.

[0010] In some embodiments, the impedance is provided by the parasitic impedance. In various other embodiments, the impedance is separate from the parasitic impedance.

[0011] In various embodiments, the gain of the amplifier is selected to be substantially equal to 1.

[0012] In some embodiments, the method further comprises selecting the gain and the compensation impedance such that the compensation current magnitude is substantially equal to the leakage current magnitude.

[0013] The active guarding circuit as defined in claim 4, wherein the gain and the compensation impedance are selected so that the compensation current magnitude is substantially equal to the leakage current magnitude.

[0014] In some embodiments, the gain of the amplifier is selected to be greater than 1.

[0015] In various embodiments, the impedance includes a capacitance. In various embodiments, the impedance includes a resistance. In some embodiments, the impedance includes both a resistance and a capacitance. In various other embodiments, the impedance is a capacitance. In some other embodiments, the impedance is a resistance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The skilled person in the art will understand that the drawings, described below, are for illustration purposes only. The drawings are not intended to limit the scope of the applicants' teachings in any way.

[0017] FIG. 1 is a schematic diagram of a signal-transmission channel having a parasitic impedance;

[0018] FIG. 2 is a schematic diagram of a portion of a circuit with several sources of parasitic impedances indicated;

[0019] FIGS. 3 to 8 are schematic diagrams of active guarding circuits according to various embodiments of applicants' teachings; and

[0020] FIG. 9 is a schematic diagram of a portion of a circuit illustrating the application of active guarding circuits according to various embodiments of applicants' teachings.

DETAILED DESCRIPTION

[0021] Signals that are transmitted over signal-transmission channels can be attenuated or otherwise distorted. One reason for such distortion and attenuation is that signal-transmission channels often have parasitic impedances coupled to them. FIG. 1 illustrates a circuit **100** that comprises a signal-transmission channel **182** that is shunted by a parasitic impedance **184**. Such parasitic impedances may be resistive or capacitive or a combination of the two. The exact value of the parasitic impedance is in part determined by the frequency of the signal passing through the impedance.

[0022] As illustrated in Figure 1, a parasitic impedance may provide a signal with an alternate path to ground. In short, such a parasitic impedance forms a voltage divider with any other load that is coupled to the signal-transmission channel. In this manner, the presence of parasitic impedance may cause attenuation and/or distortion of the signal.

[0023] Parasitic impedances can arise from a wide variety of sources including but not limited to other signal-transmission channels, other circuit components, and shielding. FIG. 2 illustrates a number of sources of parasitic impedances. Specifically, FIG. 2, is a schematic diagram of a portion of a circuit having a signal-transmission channel **282**, several parasitic impedances **284a** to **284b**, shield **290**, and a multiplexer **292**.

[0024] Shield **290** runs parallel to signal-transmission channel **282** and thereby causes parasitic impedances **284a** and **284b** to exist between signal-transmission channel **282** and shield **290**. Similarly, parasitic impedances **284c** and **284d** exist between the input of the multiplexer and the power supplies of the multiplexer. FIG. 2 is intended to be illustrative only. Parasitic impedances may exist for a variety of reasons. In addition, although FIG. 2

only illustrates capacitive impedances, the impedances may also be resistive or a combination of resistive and capacitive.

[0025] Thus, parasitic impedances may exist in various forms for a variety of reasons in commonly used circuits. The presence of parasitic impedances can cause the signals that are transmitted by these circuits to be attenuated or otherwise distorted. The circuits and methods according to applicant's teachings can be used to minimize or eliminate the negative effects caused by parasitic impedances.

[0026] In various embodiments, applicants' teachings are related to an active guarding circuit and method for reducing impedance signal loading. Further, in some embodiments, applicants' teachings are related to a circuit and method for reducing capacitive signal loading. Moreover, in other embodiments, applicants' teachings are related to a circuit and method for reducing resistive signal loading. Furthermore, in some embodiments, applicants' teachings are related to a circuit and method for reducing resistive and capacitive signal loading. In yet other embodiments, applicants' teachings are related to an active guarding circuit and method for reducing impedance signal loading with an adjustable control of level compensation. Applicants' teachings are not intended to be limited to the above-described embodiments.

[0027] Reference is now made to FIG. 3, which is schematic diagram of an active guarding circuit **300** according to various embodiments of applicants' teachings. Circuit **300** can be created by adding an amplifier **310** and a compensation impedance **380** to the circuit **100** of FIG. 1. More specifically, the input of the amplifier **310** is coupled to the signal-transmission channel **382** and the output is coupled to one terminal of the compensation impedance **380**. The other terminal of the compensation impedance is coupled to the signal-transmission channel **382**. Parasitic impedance **384** has one terminal **385a** connected to signal-transmission channel **382** and a second terminal **385b** connected to ground. The terminal of a parasitic impedance, such as terminal **385b**, that is not connected to the signal transmission channel of interest, will be referred to as the termination point of

the parasitic impedance. The ground node may include but is not limited to small signal ground, such as a power supply terminal.

[0028] Compensation impedance **380** and parasitic impedance **384** may be any appropriate impedance including but not limited to a resistance, a capacitance or any appropriate combination, whether in series or parallel, of resistance and capacitance.

[0029] Signal-transmission channel **382** may be used to transmit a signal to a load (not shown), which may be any suitable circuit or circuit component. The presence of a signal on signal-transmission channel **382** causes a voltage to appear across parasitic impedance **384**. This causes a leakage current $I_{leakage}$ to flow through the parasitic impedance **384**. The magnitude of the current flowing through parasitic impedance **384** depends on the value of the impedance as well as the magnitude of the voltage appearing across its terminals.

[0030] Amplifier **310** amplifies the signal appearing on the signal-transmission channel **382**. In various embodiments amplifier **310** has a gain that is greater than 1. This causes a voltage to appear across compensation impedance **380** and a current I_{comp} to flow through compensation impedance **380**.

[0031] In various embodiments, the gain of amplifier **310** and the value of the compensation impedance is selected such that the current that flows through parasitic impedance **384** is compensated for by the current that flows through compensation impedance **380**. Specifically, given a signal voltage of V_{signal}, a parasitic impedance of Z_{para}, the leakage current can be said to be:

[0032] $$I_{leakage} = V_{signal} \times \left(\frac{1}{Z_{para}} \right) \qquad \text{Equation (1)}$$

[0033] Similarly, given a compensation impedance of Z_{comp} and an amplifier gain of G, the compensation current flowing through the compensation impedance may be said to be:

[0034] $$I_{comp} = V_{signal} \times (G-1) \times \left(\frac{1}{Z_{comp}}\right)$$ Equation (2)

[0035] Equating equation (1) and equation (2) yields the following:

[0036] $I_{comp} = I_{leakage}$

[0037] $$\left(\frac{G-1}{Z_{comp}}\right) = \frac{1}{Z_{para}}$$ Equation (3)

[0038] Thus, by selecting G and Z_{comp} to satisfy equation (3) the compensation current will exactly match the leakage current. The compensation impedance **380** effectively serves as a negative impedance that cancels the effect of the parasitic impedance **384**.

[0039] In various embodiments, the value of the parasitic impedance may not be known and therefore it may not be possible to select a gain for the amplifier by simply using equation (3) above. In such embodiments, the value of the gain can be estimated by using circuit **300** of FIG. 3. Specifically, circuit **300** is implemented by selecting a compensation impedance and range of values of gain. The circuit is operated at the various values of gain and the output is monitored. For those values of gain that exceed the required value, the output would oscillate. Thus, the correct value of the gain lies in a range of values that is bounded by (1) the lowest known value of the gain at which the output oscillates and (2) the highest known value of the gain at which the output does not oscillate. This process may be continued in an iterative manner until a suitable value of gain is selected. Once an appropriate value of gain is determined, the parasitic impedance may be estimated by using equation (3) given above.

[0040] In various embodiments, the parasitic impedance may be comprised of both parasitic and resistive elements. However, in some embodiments the effect of the capacitive loading can be significantly greater than the effect of the resistive loading. In such cases, various embodiments of applicants' teachings may be used to address the capacitive loading and not

the resistive loading. Alternatively, applicants' teachings may be used to partially compensate for any portion of the parasitic impedance. Thus, in various embodiments, circuits according to applicants' teachings may be used to reduce and/or partially compensate for any leakage currents that may flow through any parasitic impedances coupled to a signal-transmission channel, but not necessarily to completely compensate for all the current that is lost due to leakage currents.

[0041] Alternatively, the parasitic impedance may be measured or estimated according to known techniques. The value of the parasitic impendence obtained from this may then be used to select initial values for the compensation impedance and the range of values of gain. The gain can then be fine tuned according to the above-described method.

[0042] Reference is next made to FIG. 4, which is a schematic diagram of an active guarding circuit **400** according to various embodiments of applicants' teachings. Circuit **400** may be created by applying the output of amplifier **410** to the termination point of parasitic impedance **484**. Specifically, in some applications, the termination point, or terminal **485b** of parasitic impedance **484** of FIG. 4 may be accessible. In such instances, it may be possible to connect the output of an amplifier to terminal **485b** of parasitic impedance **484** and therefore, it may not be necessary to utilize a circuit with a separate compensation impedance.

[0043] Circuit **400** can be implemented by connecting the input of amplifier **410** to signal-transmission channel **482** and the output of amplifier **410** to the terminal of the parasitic impedance **484** that is not connected to signal-transmission channel **482**.

[0044] Signal-transmission channel **482** may be used to transmit a signal to a load, which may be any suitable circuit or circuit component (not illustrated). The presence of a signal on signal-transmission channel **482** causes a voltage to appear across parasitic impedance **484**. This causes a leakage current to flow through the parasitic impedance **484**. The magnitude

of the current flowing through parasitic impedance **484** depends on the value of the impedance as well as the magnitude of the voltage appearing across its terminals.

[0045] Amplifier **410** amplifies the signal appearing on the signal-transmission channel **482** and applies the amplified signal to the terminal of parasitic impedance **484** that is not connected to the signal-transmission channel **482**. This causes a compensation current to flow through the parasitic impedance **484**. In various embodiments, the gain of amplifier **410** is selected to be substantially equal to 1. In such a case, the voltage appearing at the terminal of parasitic impedance **484** that is connected to the output of amplifier **410** is substantially equal to the voltage appearing at the opposite terminal of parasitic impedance **484** thereby causing a compensation current, having an equal magnitude but opposite direction to the leakage current, to flow through parasitic impedance **484**. Since the currents are equal in magnitude but opposite in direction, they cancel each other and no current flows through the parasitic impedance **484**. Stated another way, a substantially equal voltage potential exists at either terminal of parasitic impedance **484** therefore, no substantial current flows through the parasitic impedance **484**.

[0046] As shown in the illustrative example of FIG. 4, parasitic impedance **484** serves as both a parasitic impedance and a compensation impedance. Thus, where terminal **485b** of parasitic impedance **484** may be accessed, a more simple compensation circuit may be achieved than may be possible when terminal **485b** is not accessible. In particular, a separate compensation impedance is not necessary and the gain of the amplifier may be set to 1.

[0047] Moreover, in various embodiments, circuit **400** may be utilized without knowing the value of parasitic impedance. In addition, if extra compensation is required, then the gain of the amplifier may be appropriately adjusted as will be explained in greater detail below.

[0048] Reference is now made to FIG. 5, which is a detailed schematic diagram of an active guarding circuit **500** according to various embodiments of applicants' teachings. Specifically, circuit **500** may be utilized to implement circuits equivalent to either circuit **300** or **400** as will be explained in greater detail below.

[0049] Circuit **500** comprises an amplifier portion **510** which in turn comprises an operational amplifier **512** with a non-inverting input **514**, an inverting input **516**, an output node **517**, and power rails **518** and **520**.

[0050] Circuit **500** also comprises input node **522**, guarding output **524** and negative impedance output **526**. More specifically, input node **522** is the node that is connected to a signal-transmission channel. Guarding output **524** is the output utilized when using a configuration similar to that illustrated in FIG. 4. Specifically, if the termination point of a parasitic capacitance is accessible, then guarding output **524** may be used to connect to the termination point of the parasitic impedance. In contrast, negative impedance output **526** is the output that is used to connect to a signal-transmission channel when the termination point of the parasitic impedance is not accessible.

[0051] Referring again to the amplifier portion **510**, amplifier portion **510** further comprises an input balancing portion **528**, a gain control portion **530**, and a stability control portion **532**. Input balancing portion **528** comprises resistor **534**. Gain control portion comprises resistor **536**, one terminal of which is connected to ground **538**, and resistor **540**. By adjusting the values of resistors **536** and **540**, one is able to adjust the gain G of the overall amplifier portion **510**. In some embodiments, when negative impedance output **526** is utilized the values of resistors **536** and **540** may be set to a value that is greater than 1. In various other embodiments, when guarding output **524** is utilized, the values of resistors **536** and **540** may be selected to provide a gain of greater than 1. Stability control portion **532** comprises capacitor **542**, resistor **544**, and resistor **546**. By adjusting the values of capacitor **542**,

resistor **544**, and resistor **546** one is able to alter the stability of the overall amplifier circuit.

[0052] Circuit **500** can also comprise compensation level portion **580**, when used in a configuration similar to FIG. 3. Compensation level portion **580** is in turn comprised of resistor **546** and capacitor **548**. Compensation level portion **580** is used as the compensation impedance. By adjusting gain control portion **530** and compensation level portion **582**, one may adjust the compensation current that is provided to the signal-transmission channel, and thereby match the compensation current magnitude to the magnitude of the leakage current. This may be done according to equation (3) given above. It should be understood however, that in various embodiments, where circuit 500 is used in a configuration similar to FIG. 4, compensation level portion **580** and output **526** can be omitted.

[0053] Reference is now made to FIG. 6, which is a detailed schematic diagram of an active guarding circuit **600** according to various embodiments of applicants' teachings. Circuit **600** comprises amplifier **610**, which is coupled to compensation impedance **680**. Both amplifier **610** and compensation impedance **680** are coupled to signal path **682**, which has parasitic impedance **684**. Parasitic capacitance **684** may be comprised of various impedances such as capacitances **686** and **688**, which may be distributed throughout the signal-transmission channel **682**. Parasitic capacitances 686 and 688 have termination points **685b**. Both compensation impedance **680** and parasitic impedance **684** are illustrated as only containing capacitances. However, it is not intended to exclude embodiments in which compensation impedance **680** and parasitic impedance **684** include resistances or a combination of capacitances and resistances, which may appear as some combination of parallel or serial connections.

[0054] Amplifier **610**, comprises an operational amplifier **612**, with a non-inverting input **614**, an inverting input **616**, an output node **617**, and power rails **618** and **620**. Amplifier **610** further comprises resistor **634** connected between the non-inverting input **614** and signal-transmission

channel **682**. Resistor **636**, which is connected between ground **638** and inverting input **616**, as well as resistor **640**, form a gain control portion. In various embodiments, the values of resistors **636** and **640** are selected to have a gain with a value greater than 1. Capacitor **642**, resistor **644** and resistor **646** form a stability control portion.

[0055] Capacitors **648** and **650** make up a compensation impendence **680** and are connected between resistor **646** and signal-transmission channel **682**. As discussed above, the value of compensation impedance and the gain of the amplifier may be selected according to equation (3) in order to cancel or reduce the effect of the parasitic impedance and the leakage current.

[0056] Reference is next made to FIG. 7, which is a detailed schematic diagram of an active guarding circuit **700** according to various embodiments of applicants' teachings. Circuit **700** is illustrated with specific values for various circuit components indicated. Circuit **700** may be utilized to compensate for parasitic capacitance **784** that has a value of 90 pF and appears across a signal-transmission channel **782**.

[0057] Circuit **700** comprises amplifier **710**, which is coupled to compensation impedance **780**. Both amplifier **710** and compensation impedance **780** are coupled to the signal-transmission channel **782**. The parasitic capacitance **784** could be distributed throughout the signal-transmission channel **782** and be made up of various impedances such as capacitances **786** and **788** having termination points **785b**.

[0058] Amplifier **710**, comprises an operational amplifier **712**, which may be, but is not limited to being, implemented as an U21 LMH6642 operation amplifier. Operational amplifier **712** has a non-inverting input **714**, an inverting input **716**, an output node **717**, and power rails **718** and **720**. Amplifier **710** further comprises resistor **734** connected between the inverting input **714** and signal-transmission channel **782**. Resistor **736** has a value of 100 kΩ and is connected between ground **738** and inverting input **716**.

Resistor **740** has a value of 10 kΩ and is connected in parallel with capacitor **742**. Resistors **738** and **740** form a gain control portion.

[0059] Capacitor **742** and resistor **746** form a stability control portion. Capacitor **742** has a value of 10 pF, and resistor **746** has value of 100 Ω.

[0060] Capacitors **748** and **750** make up a compensation impendence **780** and are connected between resistor **746** and signal-transmission channel **782**.

[0061] Circuit **700** may be utilized when the termination point of the parasitic impedance is not readily accessible. Specifically, it may not be possible to connect the output of amplifier **710** to terminal **785b** of parasitic impedance **784**.

[0062] Reference is next made to FIG. 8, which is a detailed schematic diagram of an active guarding circuit **800** according to various embodiments of applicants' teachings. Circuit **800** comprises amplifier **810**, the input of which is coupled to signal-transmission channel **882**. Signal-transmission channel **882** has parasitic impedance **884**. Parasitic impedances **884** may be comprised of various impedances such as capacitances **886** and **888**, which may be distributed through out the signal-transmission channel **882**. Although parasitic impedance **884** is illustrated of being comprised of only capacitances, it is not intended to exclude embodiments in which parasitic impendence **884** is comprised of resistors, or a combination of resistive and capacitive elements.

[0063] The output of amplifier **810** is coupled to node **885b** of parasitic impedance **884**. Node **885b** corresponds to the termination point of parasitic capacitance **884**.

[0064] Amplifier **810**, comprises an operational amplifier **812**, with a non-inverting input **814**, an inverting input **816**, an output node **817**, and power rails **818** and **820**. Amplifier **810** further comprises resistor **834** connected between the inverting input **814** and signal-transmission channel **882**. Resistor **836**, which is connected between ground **838** and inverting

input **816**, as well as resistor **840**, form a gain control portion. Capacitor **842**, resistor **844** and resistor **846** form a stability control portion.

[0065] Circuit **800** may be utilized when the termination point, or terminal **885b**, of the parasitic impedance **884** is readily accessible. Specifically, the output of amplifier **810** is connected to terminal **885b** of parasitic impedance **884**.

[0066] The use of any circuit components such as amplifiers may introduce delays into circuits. If the delay is significant then the circuit may not adequately compensate for any leakage current that is lost through the parasitic impedance. This may result in signal distortion. Various embodiments of the circuits illustrated above may overcome the difficulties associated with delays by utilizing amplifiers with a sufficient bandwidth so as not to introduce a delay that is significant when compared to the bandwidth of the signal that is propagated over the signal-transmission channel.

[0067] For example, various embodiments of the circuits illustrated above may make use of an operational amplifier when implementing the amplifier for the signal. In some embodiments, the bandwidth of the operational amplifier, such as operational amplifier **812** is selected to be at least 10 times the bandwidth of the signal being propagated over the signal transmission channel. In various embodiments, the signal that is propagated on the signal-transmission channel is a sinusoidal signal. In such cases, the bandwidth of the signal is simply the frequency of the signal, and the bandwidth of the amplifier may be appropriately selected.

[0068] An alternative solution for compensating for delay is that a phase lead of an appropriate signal may be added to the amplifier of any of the above signals. This requires that the circuit be able to predict the future values of the signal. In the case of sinusoidal signals, or any other periodic signal, this may be accomplished very easily as the value of such a signal may always be predicted for any future time.

[0069] Reference is now made to FIG. 9, which is a schematic diagram of a circuit **900** according to various embodiments of applicants' teachings. Specifically, FIG. 9, illustrates the application of active guarding circuits according to applicants' teachings to a circuit similar to that illustrated in FIG. 2.

[0070] Illustrated in FIG. 9 is a signal-transmission channel **982**, several parasitic impedances **984a** to **984d**, shield **990**, and a multiplexer **992**. Shield **986** runs parallel to signal-transmission channel **982** and thereby causes parasitic impedances **984a** and **984b** to exist between signal-transmission channel **982** and shield **986**. Similarly, parasitic impedances **984c** and **984d** exist between the input of the multiplexer and the power supplies of the multiplexer.

[0071] Amplifiers **910a**, **910b**, and **910c** are utilized to compensate for any leakage current that may occur. Specifically, the inputs of amplifiers **910a**, **910b**, and **910c** are coupled to the signal-transmission channel and the outputs of amplifiers **910a**, **910b**, and **910c** are coupled to the termination point of impedances **984a** to **984d**. Each of the amplifiers **910a**, **910b**, and **910c** may be implemented as discussed with respect to FIGS. 4 and 8.

[0072] Although FIG. 9 only illustrates capacitive impedances, the impedances may also be resistive or may be any combination of resistances and capacitances connected in series or parallel. It is not intended to exclude any of these combinations. FIG. 9 is intentionally simplified for the purposes of clarity of illustration.

[0073] While the applicants' teachings are described in conjunction with various embodiments, it is not intended that the applicants' teachings be limited to such embodiments. On the contrary, the applicants' teachings encompass various alternatives, modifications, and equivalents, as will be appreciated by those of skill in the art.

WE CLAIM:

1) An active guarding circuit for reducing parasitic impedance signal loading, the circuit comprising:

a signal-transmission channel that carries an electrical signal and is shunted by a parasitic impedance having a parasitic impedance value, the electrical signal causes a leakage current having a leakage current magnitude to flow through the parasitic impedance;

an impedance having an impedance value, a first terminal and a second terminal, the first terminal coupled to the signal-transmission channel; and

an amplifier having an input terminal, an output terminal and a gain, the input terminal coupled to the signal-transmission channel, the output terminal coupled to the second terminal of the impedance to provide a compensation current to flow through the impedance, and the gain is selected based on the impedance and parasitic impedance values so that the compensation current has a magnitude substantially equal to the leakage current magnitude.

2) The active guarding circuit as defined in claim 1, wherein the impedance is the parasitic impedance.

3) The active guarding circuit as defined in claim 1, wherein the gain is substantially equal to 1.

4) The active guarding circuit as defined in claim 1, wherein the impedance is separate from the parasitic impedance.

5) The active guarding circuit as defined in claim 4, wherein the gain and the compensation impedance are selected so that the compensation current magnitude is substantially equal to the leakage current magnitude.

6) The active guarding circuit as defined in claim 4, wherein the gain is greater than 1.

7) The active guarding circuit as defined in any of the claims 1 to 6, wherein the impedance includes a capacitance.

8) The active guarding circuit as defined in any of the claims 1 to 6, wherein the impedance includes a resistance.

9) The active guarding circuit as defined in any of the claims 1 to 6, wherein the impedance includes both a resistance and a capacitance.

10) The active guarding circuit as defined in any of the claims 1 to 6, wherein the impedance is a capacitance.

11) The active guarding circuit as defined in any of the claims 1 to 6, wherein the impedance is a resistance.

12) A method of active guarding for reducing parasitic impedance signal loading, the method comprising:

sensing an electrical signal on a signal-transmission channel, the signal-transmission channel is shunted by a parasitic impedance having a parasitic impedance value, the electrical signal causing a leakage current having a leakage current magnitude to flow through the parasitic impedance;

providing an impedance having an impedance value, with a first terminal and a second terminal, the first terminal is coupled to the signal-transmission channel;

providing an amplified signal to the second terminal of the impedance to cause a compensation current to flow through the impedance, the amplified signal is equal to the electrical signal multiplied by a gain, the gain is selected based on the impedance value and the parasitic impedance value so that the magnitude of the compensation current is substantially equal to the leakage current magnitude.

13) The method as defined in claim 12, wherein the impedance is provided by the parasitic impedance.

14) The method as defined in claim 12, wherein the gain is selected to be equal to 1.

15) The method as defined in claim 12, wherein the impedance is separate from the parasitic impedance.

16) The method as defined in claim 15, further comprising selecting the gain and the compensation impedance such that the compensation current magnitude is substantially equal to the leakage current magnitude.

17) The method as defined in claim 15, wherein the gain is selected to be greater than 1.

18) The method as defined in any of the claims 12 to 17, wherein the impedance includes a capacitance.

19) The method as defined in any of the claims 12 to 17, wherein the impedance includes a resistance.

20) The method as defined in any of the claims 12 to 17, wherein the impedance includes both a resistance and a capacitance.

21) The method as defined in any of the claims 12 to 17, wherein the impedance is a capacitance.

22) The method as defined in any of the claims 12 to 17, wherein the impedance is a resistance.

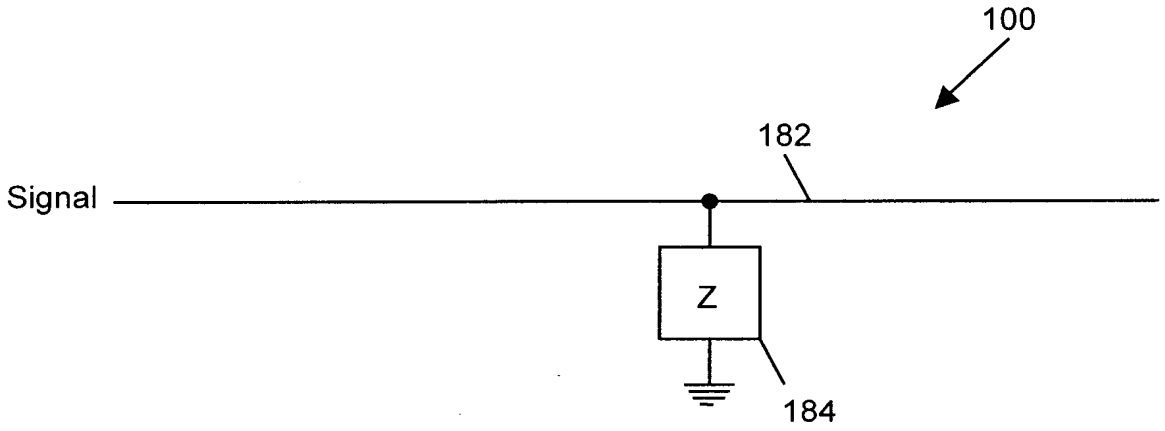

FIG. 1

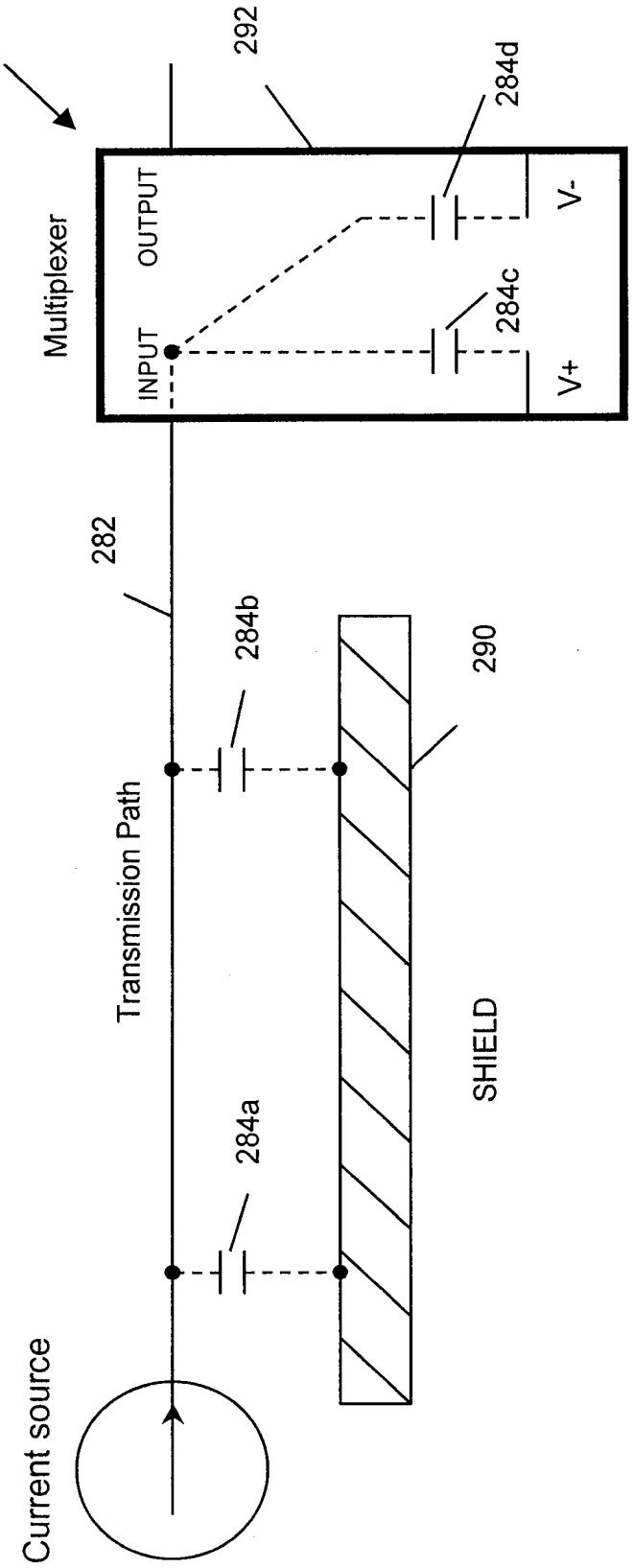
200
292
284d
Multiplexer
OUTPUT
V-
284c
INPUT
V+
282
284b
290
Transmission Path
SHIELD
284a
Current source

FIG. 2

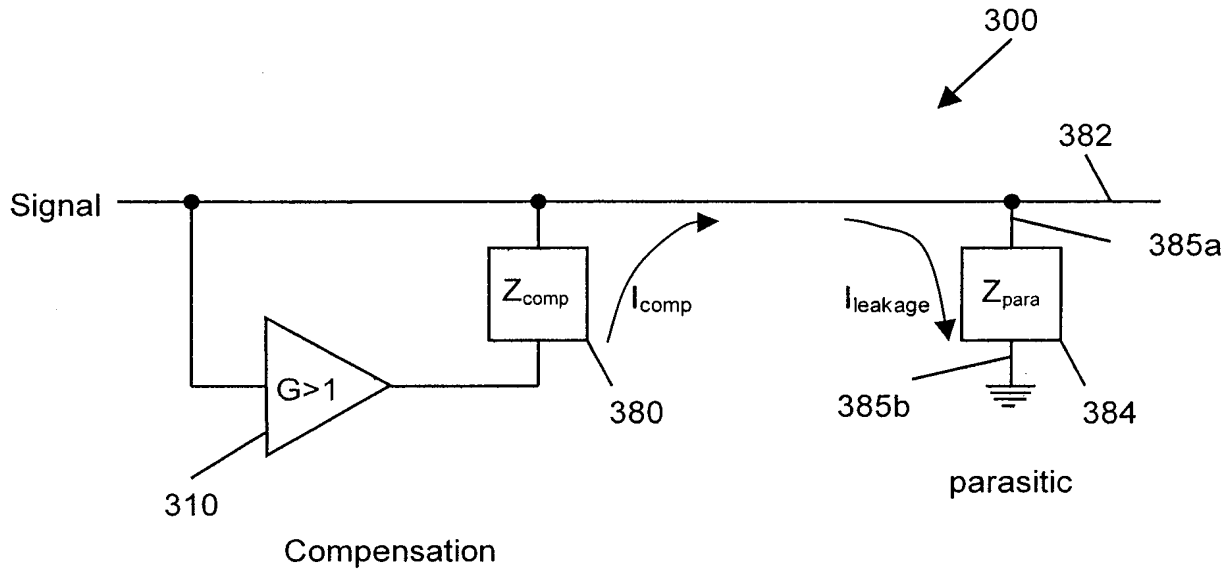
300
382
Signal
385a
Z_{comp}
I_{comp}
$I_{leakage}$
Z_{para}
G>1
380
385b
384
310
parasitic
Compensation

FIG. 3

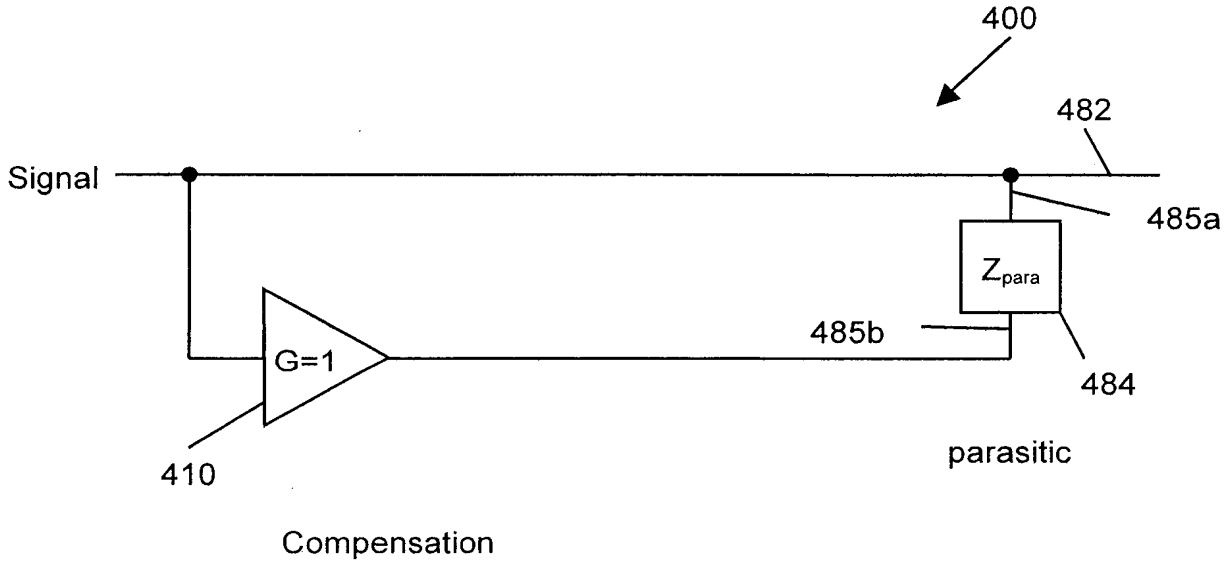
400
482
Signal
485a
Z_{para}
485b
G=1
484
410
parasitic
Compensation

FIG. 4

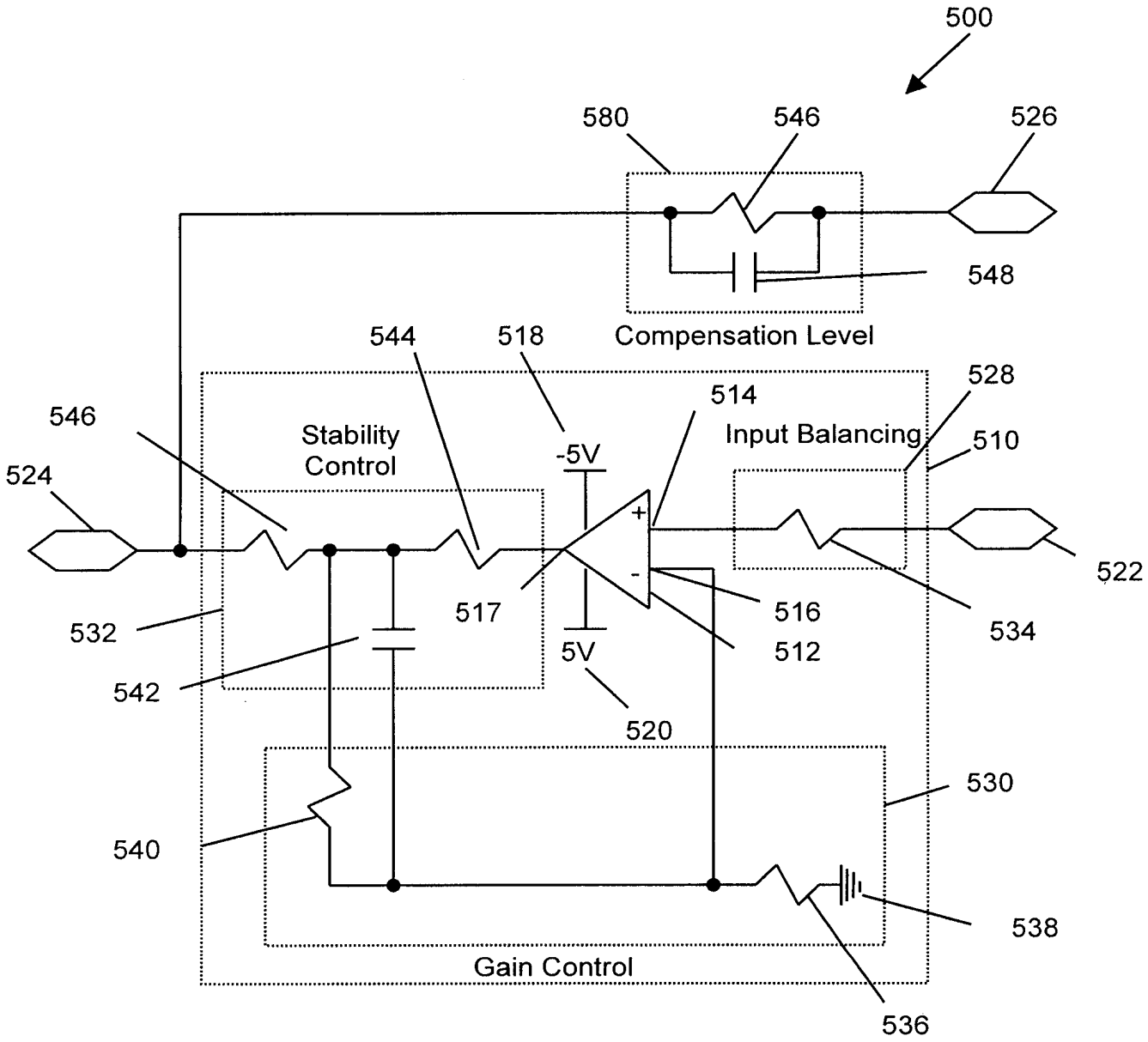
500
580
546
526
548
Compensation Level
544
518
528
514
546
Stability
Control
-5V
Input Balancing
510
524
+
-
522
517
516
532
534
512
542
5V
520
530
540
538
Gain Control
536

FIG. 5

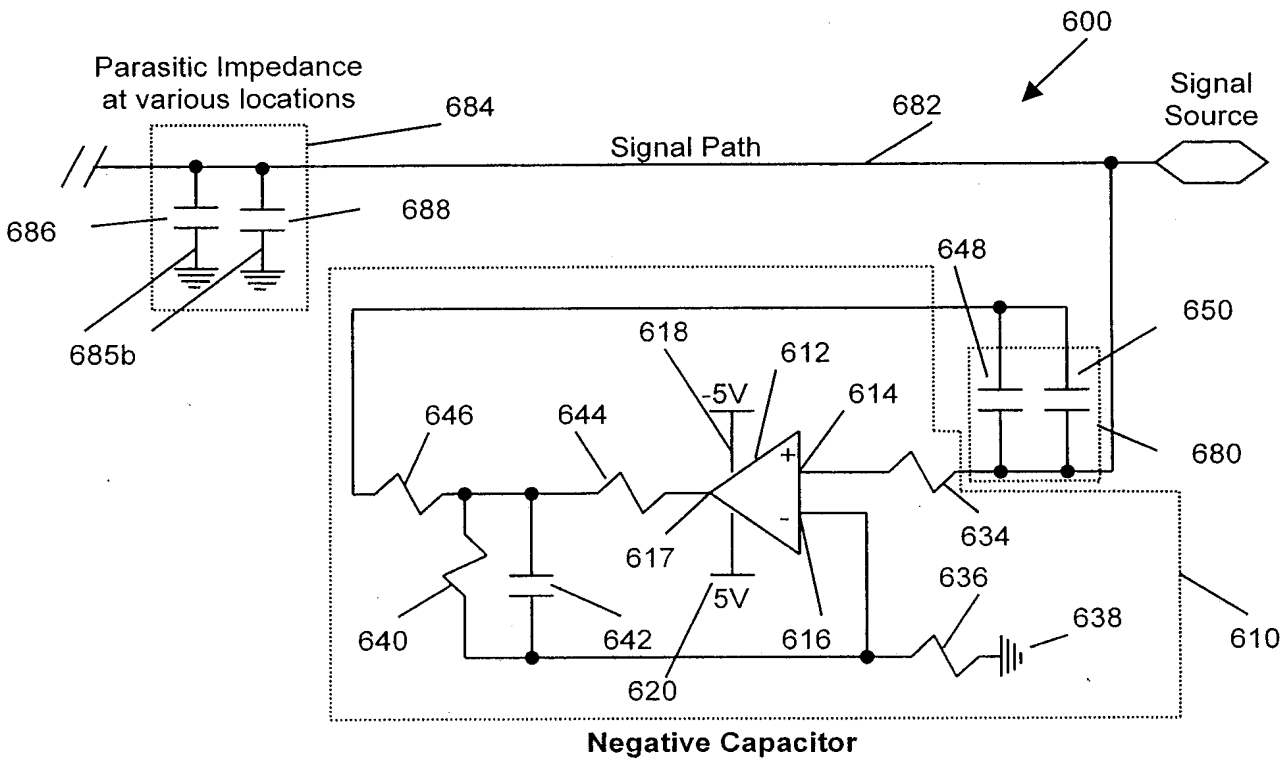
600
Parasitic Impedance
at various locations
684
682
Signal Path
Signal
Source
686
688
685b
648
650
618
612
-5V
614
646
644
680
634
617
636
638
640
642
5V
616
610
620
Negative Capacitor

FIG. 6

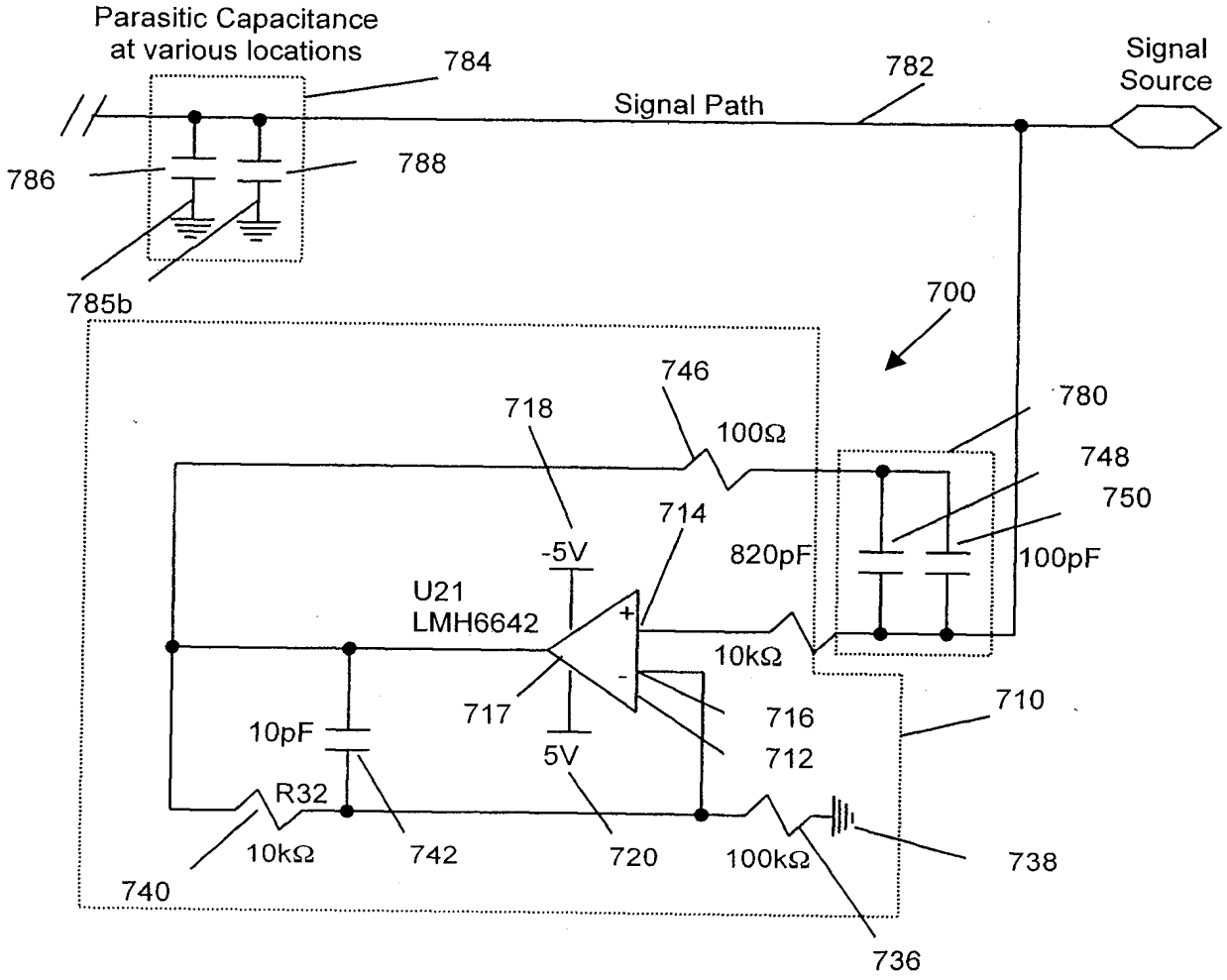
Parasitic Capacitance
at various locations
784
782
Signal Path
Signal
Source
786
788
785b
700
746
718
100Ω
780
748
750
714
-5V
820pF
100pF
U21
LMH6642
+
-
10kΩ
710
717
716
712
10pF
5V
R32
10kΩ
742
720
100kΩ
738
740
736

FIG. 7

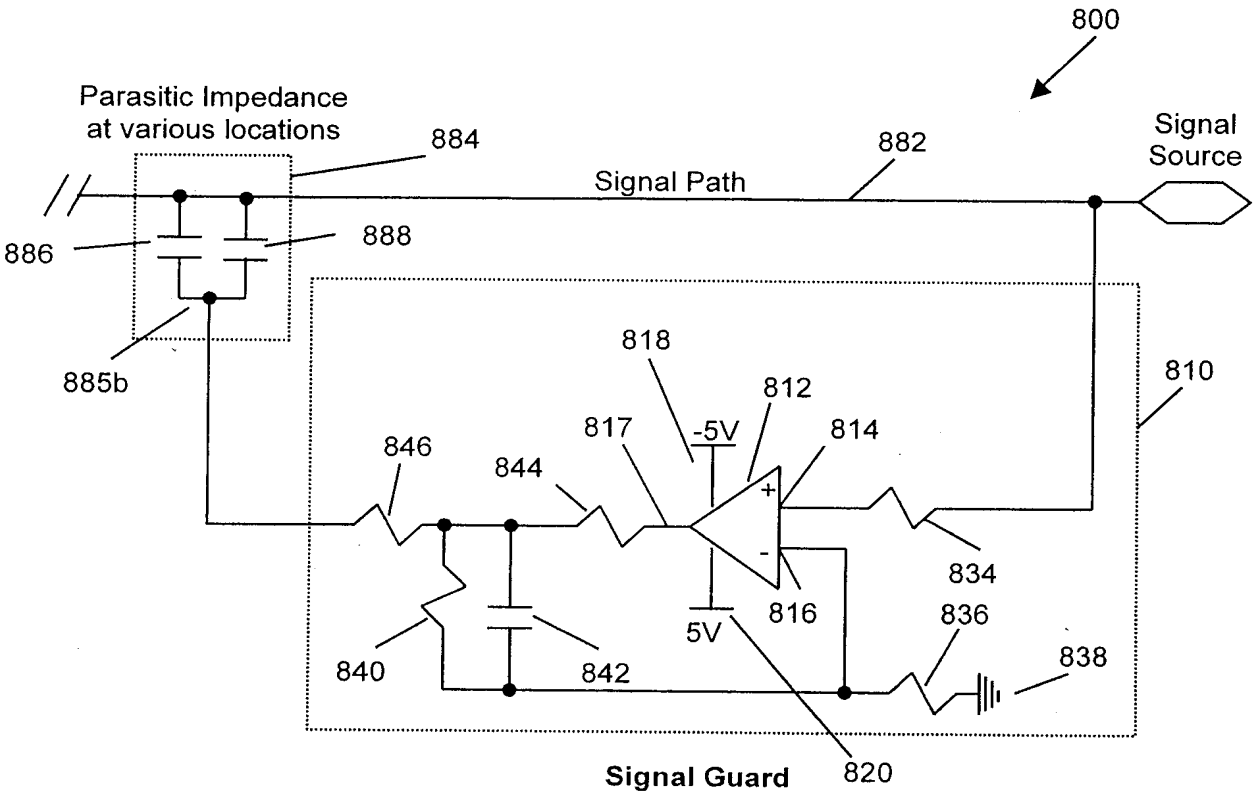
800
Parasitic Impedance
at various locations
884
882
Signal Path
Signal
Source
886
888
885b
818
812
810
817
-5V
814
846
844
+
-
834
816
836
840
842
5V
838
820
Signal Guard

FIG. 8

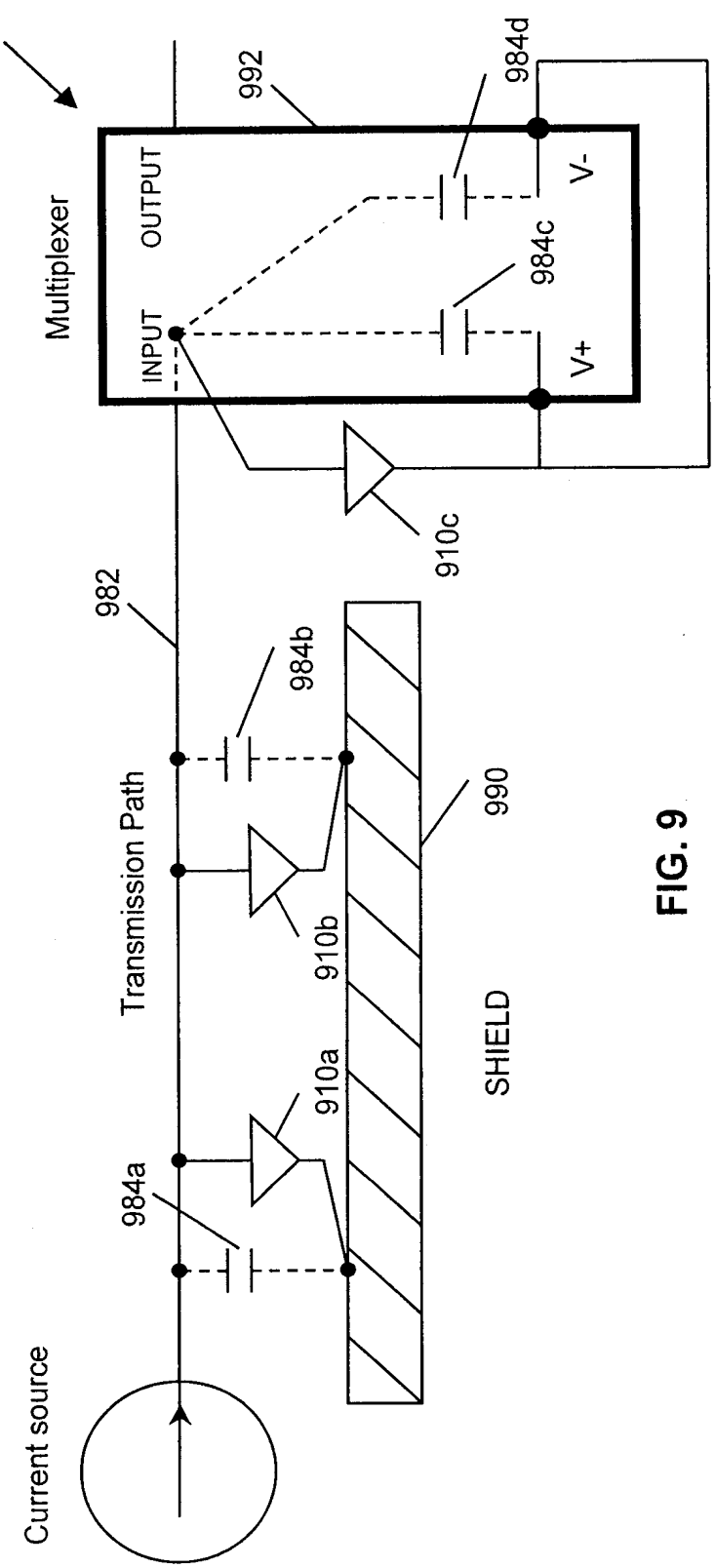
900
992
984d
Multiplexer
OUTPUT
V-
984c
INPUT
V+
910c
982
984b
Transmission Path
990
910b
910a
SHIELD
984a
Current source

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2008/000588

A. CLASSIFICATION OF SUBJECT MATTER

IPC: ***G05F 5/00*** (2006.01) , ***H03F 1/08*** (2006.01) , ***H03F 1/10*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: ***G05F 5/00*** (2006.01), ***H03F 1/08*** (2006.01), ***H03F 1/10*** (2006.01), ***G05F 1/00*** (2006.01), ***H02M 3/335*** (2006.01), ***H03L 7/093*** (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)

Databases searched: Canadian Patent Database, Delphion, European Patent Database, Abstracts of Japan, US Patent Database, WIPO- PCT Publications (Full text) and IEEE publications.

Keywords: Guarding circuit, parasitic impedance, signal-transmission, shunt*, leakage current, impedance value, amplifier or amplified, compensation current, magnitude.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006/0197509A1 (Kanamori et al.), 07 September 2006 (07-09-2006), -see abstract; -see figs. 3-7; -see whole document.	1 - 22
A	US 5,305,192 (Bonte et al.), 19 April 1994 (19-04-1994), -see abstract; -see figs. 4-9; -see whole document.	1 - 22
A	US 5,557,242 (Wetherell), 17 September 1996 (17-09-1996), -see abstract; -see figs 3-4; -see whole document	1 - 22

[ ] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 August 2008 (11-08-2008)	13 August 2008 (13-08-2008)

Name and mailing address of the ISA/CA
Canadian Intellectual Property Office
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50 Victoria Street
Gatineau, Quebec K1A 0C9
Facsimile No.: 001-819-953-2476

Authorized officer

Rajiv Agarwal
819- 997-2304

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
US 2006/0197509A1	07-09-2006	US 7242169B2	10-07-2007
US 5305192A	19-04-1994	US 5438499A	01-08-1995
US 5557242	17-09-1996	BR 9606339A WO 9637961A1	02-09-1997 28-11-1996